

84

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An Approach for Configuring Space Photovoltaic Tandem Arrays Based on Cell Layer Performance

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Introduction

Meeting solar array performance goals of 300 W/Kg requires use of solar cells with orbital efficiencies greater than 20% [ref. 1]. Only multijunction cells and cell layers operating in tandem produce this required efficiency. An approach for defining solar array design concepts that use tandem cell layers involve the following:

1. Transforming cell layer performance at standard test conditions to on-orbit performance
2. Optimizing circuit configuration with tandem cell layers
3. Evaluating circuit sensitivity to cell current mismatch
4. Developing array electrical design around selected circuit
5. Predicting array orbital performance including seasonal variations

Advanced Cell Performance Data Requirements

The accuracy of predicting on-orbit array performance is governed by the accuracy and completeness of cell layer performance data. Although acceptable performance predictions are made for Si and GaAs single layer arrays from existing data, additional cell layer performance data is required for accurate predictions of arrays with tandem cell layers. This includes spectral response and transmission as a function of environment since changes to these properties on one cell layer modify performance of other cell layers. Like Si and GaAs cells, response of tandem cell layers to radiation and other environmental conditions must be known. However, the 1 MeV electron radiation damage equivalent for Si and GaAs may be inadequate for other cell types used as a tandem cell layer, such as the electron insensitive CIS [ref. 3]. For these cell layers, another radiation methodology, such as a 1 MeV proton damage equivalent, may be needed to accurately characterize their performance.

Orbital Operating Efficiency Predictions

An early step in array design is to transform cell layer performance data reported at standard test conditions (STC) to operating performance expected at a particular orbit after a given lifetime. Performance change from STC to operating condition

is particularly significant for tandem cell layers because their use of a broader solar spectrum range results in higher solar absorptance (solar alpha) creating higher operating temperatures than single layer cells.

Single and tandem cell layers (mechanically stacked) are evaluated with performance parameters obtained from current production cells, advanced near-term cells, and future cells. Because of uncertainty and changes in reported cell performance parameters, particularly in emerging cell technologies, the analysis was conducted parametrically with respect to cell efficiency and solar absorptance. In this manner, the scope of a particular cell technology is bound between the lower capability associated with current production cells and higher capability possible with future designs.

Specific solar cells and their performance values used are listed in table 1. Additional thermal analysis parameters considered include mean solar condition (1353 W/m^2), no albedo or earth thermal load (GEO), and a 0.85 front emissivity and 0.80 rear emissivity.

By calculating operating temperatures and using temperature coefficients listed in table 1, beginning-of-life (BOL) operating efficiencies are calculated and illustrated in figure 1. In figure 1, performance boxes are shown for each cell type where the highest efficiency (upper right corner of each box) corresponds to the highest standard condition efficiency and lowest operating temperature (lowest solar absorptance). Although figure 1 shows that the on-orbit performance of most tandem cells produce higher efficiencies than single cells, the challenge to the array designer is to translate these performances into array circuits which maintain these high efficiencies.

Tandem Cell Circuit Configuration

Design analysis of tandem cell circuits will use cell layer performance data from tandem cell modules being developed jointly by Boeing and Kopin [refs. 2-5]. The tandem cell module consists of a CLEFT GaAs top cell mechanically attached to a CIS bottom cell of equal area. The mechanically stacked cell module with external interconnection to both cell layers permits a range of circuit options to be constructed. For a particular application (orbit, temperature, radiation, etc), a circuit arrangement can be selected that maximizes circuit performance by allowing full benefit of each cell type to be obtained without restricting performance of the other cell type. This is obtained in a voltage matched circuit by series connecting each cell layer type up to a common voltage compliment at which point the cell types can then be added in parallel. To evaluate performance sensitivity of circuitry options and to select the best configuration, a 10 year GEO orbit point design case is assumed.

For this case, circuit arrangements with 2 to 4 CIS cells in series for each series GaAs cell are evaluated. Table 2 lists the cell layers electrical parameters at standard test conditions (AM0, 28°C), solar alpha and temperature coefficients [ref. 6]

considered. An estimate of end-of-life (EOL) performance was obtained by examining radiation test data of these cells [ref. 3] with a 10 year radiation fluence. The fluence consists of trapped electrons and solar flare protons shielded by 2 mil CMX coverslides on the front and rear of the module. The quantity of trapped electrons was derived from ref. 7 while refs. 8 and 9 were used to obtain the solar flare proton fluence. Calculated EOL radiation degradation factors are contained in table 2.

Figure 2 illustrates the basic analysis flow used to determine the composite current vs voltage (IV) curve of the circuit from which the maximum power of the circuit is obtained.

Figure 3 illustrates the BOL and EOL circuit efficiency of each circuitry option. The horizontal lines in this figure corresponds to the sum of the peak power of the 2 cell layers. This is the maximum possible combined circuit output. The circuit arrangements produce less power because maximum power voltage (V_{mp}) of the cell layers do not match. For the 3:1 series ratio, this voltage mismatch is very slight and circuit power approaches that of the combined individual layers.

From figure 3, it can be seen that a 3 to 1 CIS to GaAs series ratio provides the highest BOL and EOL efficiency of the circuitry options. The relative softness of the series ratio sensitivity (above 2.5:1) is due to the low CIS fill factor (50%-60%) that causes a relatively flat power response over a large voltage range around its maximum power voltage point (V_{mp}). However, dropping below 2.5:1 causes a sharp drop in circuit output as the circuit V_{mp} nears the open circuit voltage (V_{oc}) of the CIS group and is no longer contributing significant power to the circuit.

Although these results show the 3:1 arrangement provides highest performance for the 10 year GEO mission, other mission environments will produce different maximum power series ratios. Because GaAs cells degrade faster than CIS [ref. 2], in a high radiation environment the series ratio shifts toward a lower number of CIS to GaAs. Whereas, larger temperature coefficients of CIS to GaAs shifts the maximum power series ratio toward a higher number of CIS to GaAs for higher operating temperature applications, such as low earth orbit (LEO). With the mechanically stacked cell assembly arrangement, near optimum series ratios can always be constructed for a given environment. However, application of this tandem cell technology to missions which experience a range of environments (such as LEO to GEO), need to shift the circuit series ratio to remain optimum or accept a performance loss during portions of its mission as the circuit remains fixed at a nonoptimum series ratio.

To examine the degree of series ratio shift in different environments, two alternative mission orbits were considered:

LEO (500 KM, 55° inclination, 5 year life),

MEO (2000 KM, 63° inclination, 5 year life)

A series ratio analysis, similar to that conducted for the GEO case, was performed for these cases with results illustrated in figures 4 and 5 (BOL and EOL respectively). From figure 4, it can be seen the optimum BOL series ratio shifts from 3:1 at GEO to 4:1 for LEO and MEO. From figure 5, the best EOL series ratio for LEO remains 4:1 because the low radiation environment has only slightly degraded the cells, while the series ratio of the high radiation MEO case has shifted from 4:1 to 3:1 as the GaAs cells have degraded significantly more than the CIS.

Cell Mismatch Impacts on Circuit Performance

With a 3:1 series ratio circuit configuration selected for the GEO application, influence individual cell layer current mismatching has on the circuit performance is evaluated. Mismatch considerations are especially a concern with high fill factor cells such as GaAs which can be forced into their reverse bias mode with only modest amount of current mismatch in the circuit.

The analysis considers an electrical circuit composed of 27 substrings in series. Each substring contains 3 GaAs cell layers in parallel and 3 CIS cell layers in series. All cell layers in the circuit were divided into 3 current categories: average, high, and low. For a given current mismatch level, current of a high cell layer equals the average current level plus the degree of mismatch, similarly for a low current cell layer. For example, with a 5% mismatch case the average, high, and low cell layers produce 1.00, 1.05, and 0.95 of the average cell layer current, respectively. These mismatched cell layers were then statistically distributed throughout the circuit.

Using BOL cell layer properties discussed previously, the composite current vs voltage (IV) curve for the circuit was calculated with the analysis flow illustrated in figure 6.

Figure 7 illustrates the circuit IV curves for mismatch cases from 0 to 5% (Si cells are typically matched to within 1.5 to 2%). Note the current range of the graph is enlarged for improved clarity. In this figure, notching of the IV curves occur as some substring elements move toward their reverse bias mode to satisfy circuit current demand. The 'x's in this figure denote voltage positions where the lowest current substring 'LLL' (containing only low cells) shifts from reverse to forward voltage bias mode. Operating this circuit at voltages below this voltage point (at a higher current level) cause this substring and its internal cells into their reverse voltage mode. Similarly, '*'s denote the position where the second lowest current substring shifts from reverse to forward voltage bias mode. To better illustrate the circuit response to mismatching, figure 8 illustrates only the 5% mismatch case and contains some of the IV curves of its substring elements.

From figure 7, power at three voltage points (V_{mp} , 87.5% V_{mp} , and 75% V_{mp}) relative to the 0% mismatch case was calculated and is illustrated in figure 9. From this figure, a 5% mismatch causes 1% loss at V_{mp} rising to 3% at 75% V_{mp} .

To prevent excessive cell layer heating caused by reverse voltage bias operation, bypass diode circuitry can be used. By limiting voltage drop in reverse voltage bias substrings to the diode voltage drop (0.9V), heating and curve notching illustrated in figures 7 and 8 are reduced. Figure 10 illustrates IV curves for the above circuit with bypass diode circuitry. Figure 11 illustrates the 5% mismatch case with some of its substrings.

Analysis of circuit sensitivity to mismatched cells, based on statistical cell layer performance, indicates the array designer must accommodate power loss and reverse bias operation of lower current cell layers during lower operating voltages if significant mismatching is present. Corrective measures include: maintaining operating voltage above critical voltage points, incorporating bypass diodes, use of cells with long term reverse bias capability, or ensuring very low mismatching occurs.

10 KW Array Electrical Design and Performance

To illustrate array performance using tandem cell layers, a BOL 10 KW (at 160V) electrical design is sized around the 3:1 circuit arrangement selected previously. Array performance was calculated from the circuit performance coupled to various array performance factors (harness loss, blocking diode voltage drop, etc) under the incident solar flux. For this study, a solar array containing a single axis tracking system in a 10° inclination orbit at GEO was assumed. These assumptions create a seasonal incident solar flux variation as illustrated in figure 12. Figure 12 also contains incident solar flux with other array assumptions (two axis tracking, etc). The varying incident solar flux modifies cell layer performance directly by changes in solar intensity and by changes in cell layer operating temperature as illustrated in figure 13. Analysis of array output at lowest solar incidence (summer solstice) determined that 123966 4 cm² tandem cell modules are required to supply 10 KW. To satisfy the operating voltage requirement of 160 volts, the modules are divided into 213 strings each with 194 substrings in series. Seasonal performance of this array is illustrated in figure 14 with IV curves for maximum and minimum solar cases illustrated in figure 15. From these figures it can be seen the 10 KW at 160V requirement is achieved.

Summary

It has been shown that advanced cell layers in tandem offer significant efficiency improvements compared to single cells in a GEO environment. An approach has been shown that combines tandem cell layers into a configuration that maximizes circuit and array performance tailored to specific mission requirements. For a 10 year GEO case, maximum circuit performance is obtained with a series ratio of 3 CIS in series for each series GaAs. Circuit current mismatch sensitivities revealed modest power loss with mild current mismatch (2-3%) and some substrings with their cell layers shifting into potentially damaging reverse voltage bias mode at lower circuit

voltages. On going efforts include near term testing of GaAs/CIS tandem cell modules in individual and circuit elements to provide additional data for refinement of array performance predictions.

References

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Table 1. Solar Cell Parameters

CELL TYPE	TEMP COEF (%/°C)	SOLAR ALPHA			TOP CELL EFFICIENCY			BOTTOM CELL EFFICIENCY UNDER		
		A	B	C	A	B	C	AlGaAs	GaAs	Si
AlGaAs	0.155	0.50	0.50	0.65	18%	17%	16%	n/a	n/a	n/a
GaAs	0.23	0.63	0.70	0.81	21%	19%	17%	4.4%	n/a	n/a
Si	0.45	0.65	0.65	0.70	16%	15%	14%	7%	2%	n/a
CIS	0.69	0.80	0.83	0.85	n/a	n/a	n/a	8%	3%	2.1%
GaSb	0.309	0.90	0.90	0.95	n/a	n/a	n/a	9.5%	4.5%	3.1%

A : POTENTIAL (FUTURE)

B: STATE-OF-THE- ART (NEAR TERM)

C: TYPICAL PRODUCTION (DEMONSTRATED OR ESTIMATED)

Table 2. Cell Layer Parameters
(1cm² 1988 balloon flight standards)

PARAMETER		SOLAR CELL TYPE		UNITS
		GaAs	CIS	
Isc		0.02993	0.01506	A
Voc		0.9818	0.3637	V
Imp		0.02885	0.01209	A
Vmp		0.8526	0.2835	V
Temp Coeff:	Isc	615	260	PPM/°C
	Voc	-2100	-4580	PPM/°C
	Imp	615	260	PPM/°C
	Vmp	-2300	-5670	PPM/°C
SOLAR ALPHA		0.78	0.83	
EOL FACTOR:	Isc	0.90	1	
	Voc	0.93	1	
	Imp	0.885	1	
	Vmp	0.885	1	

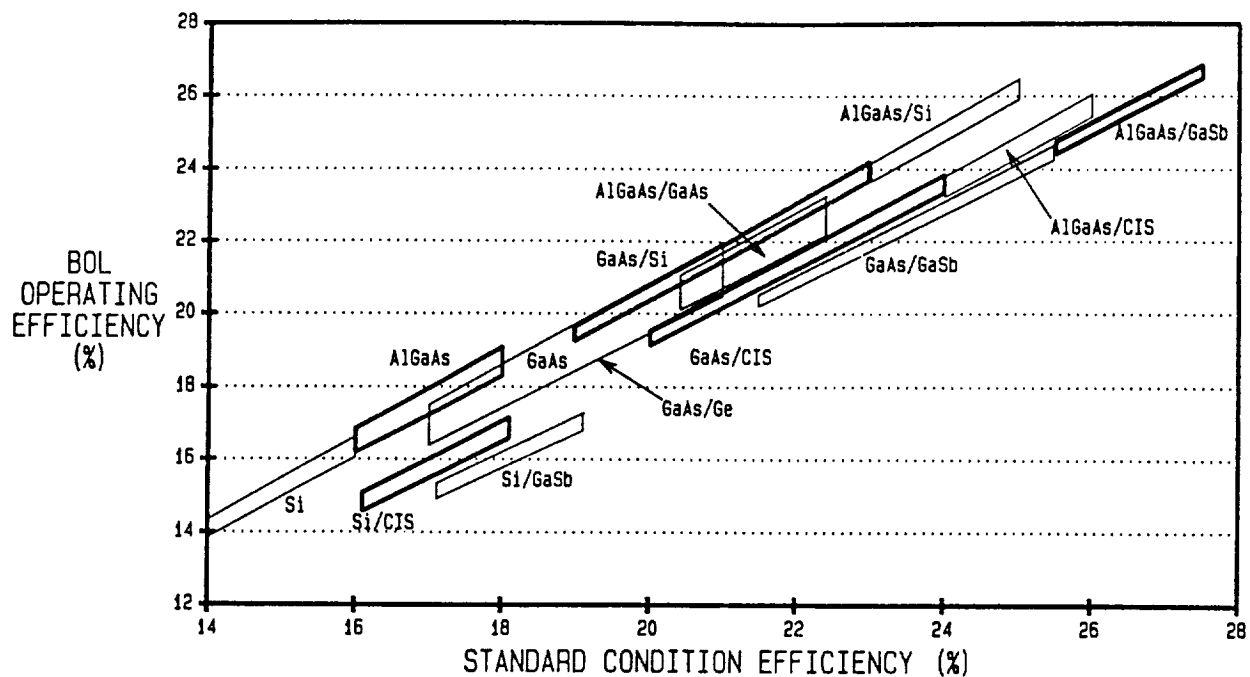


Figure 1. BOL Operating Efficiency at GEO vs Standard Test Condition Efficiency

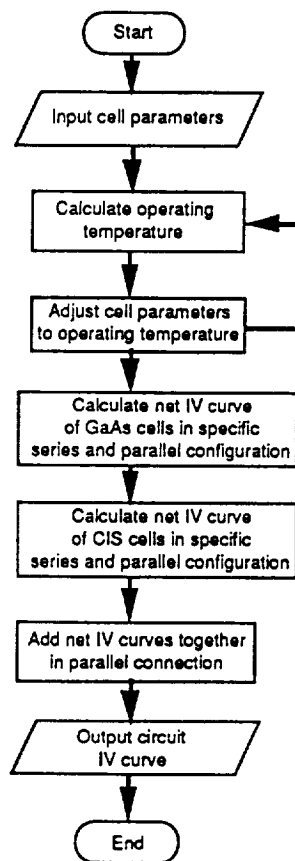


Figure 2. Algorithm Flow for Circuit Analysis Model 'IV.FOR'

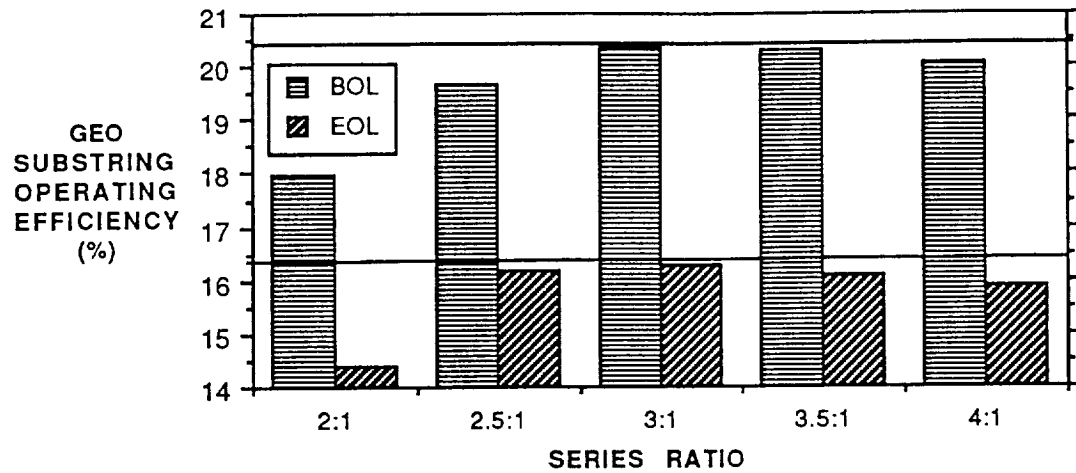


Figure 3. GEO On-orbit Circuit Sensitivity to Series Ratio

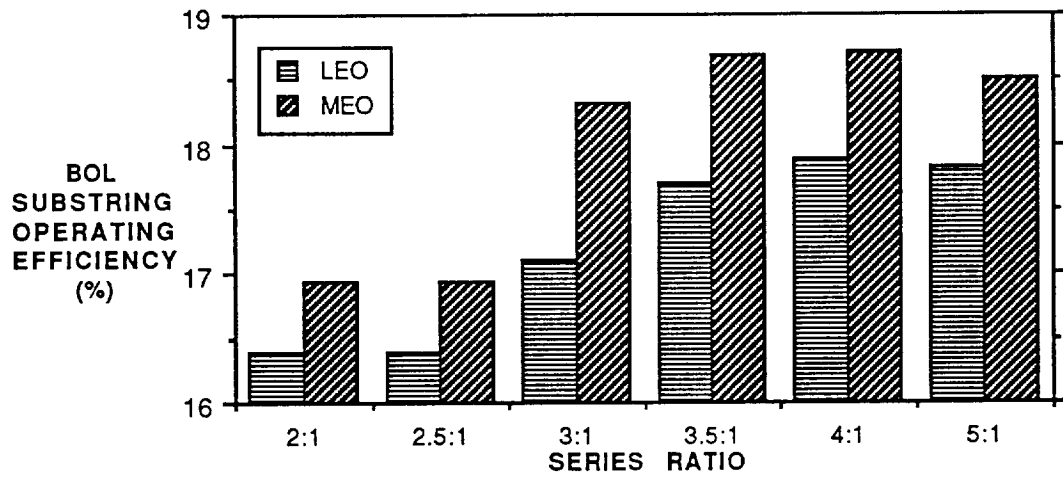


Figure 4. BOL On-orbit Circuit Sensitivity to Series Ratio

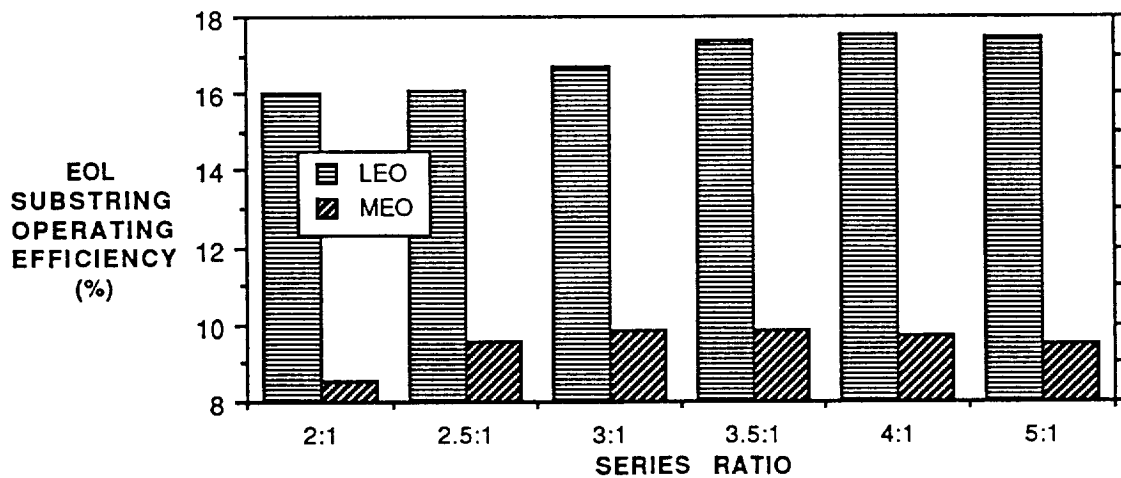


Figure 5. EOL On-orbit Circuit Sensitivity to Series Ratio

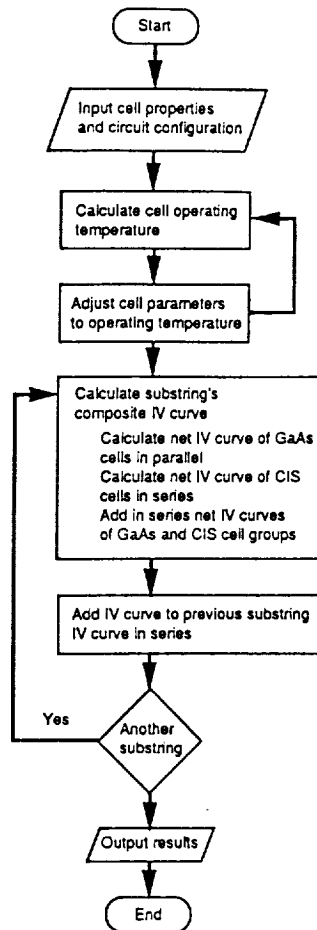


Figure 6. Algorithm Flow for Mismatch Model 'CKT.FOR'

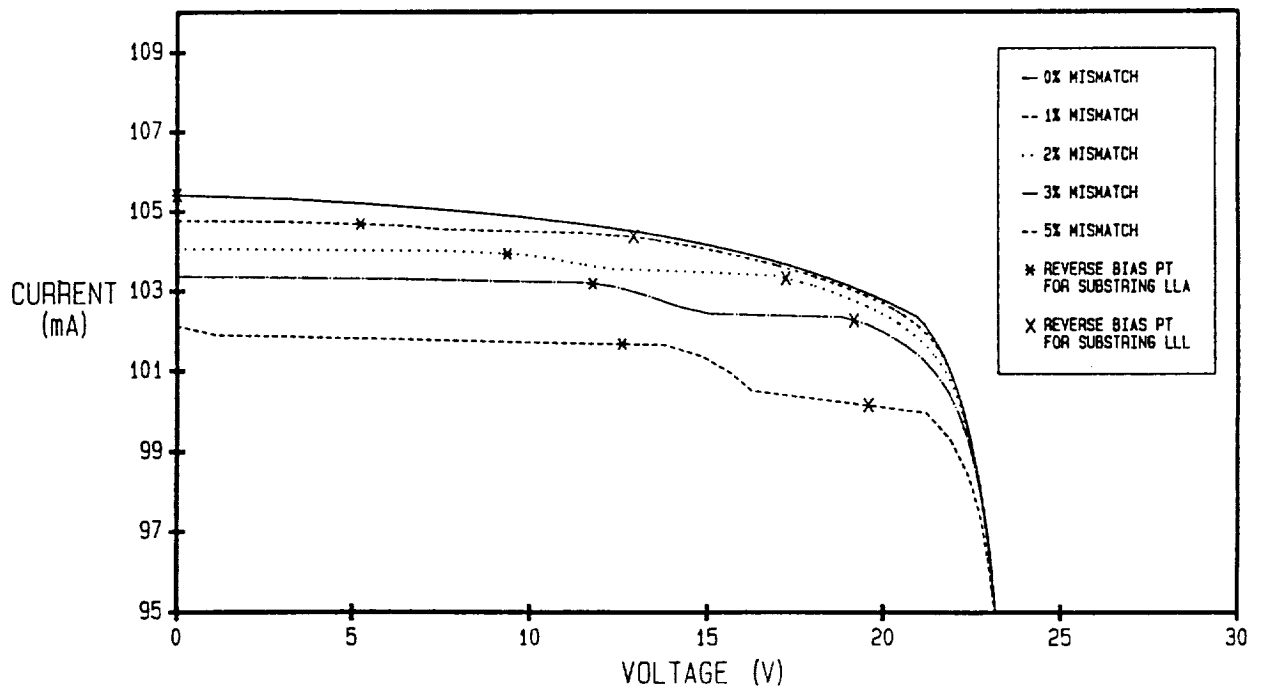


Figure 7. Circuit Sensitivity to Cell Mismatching

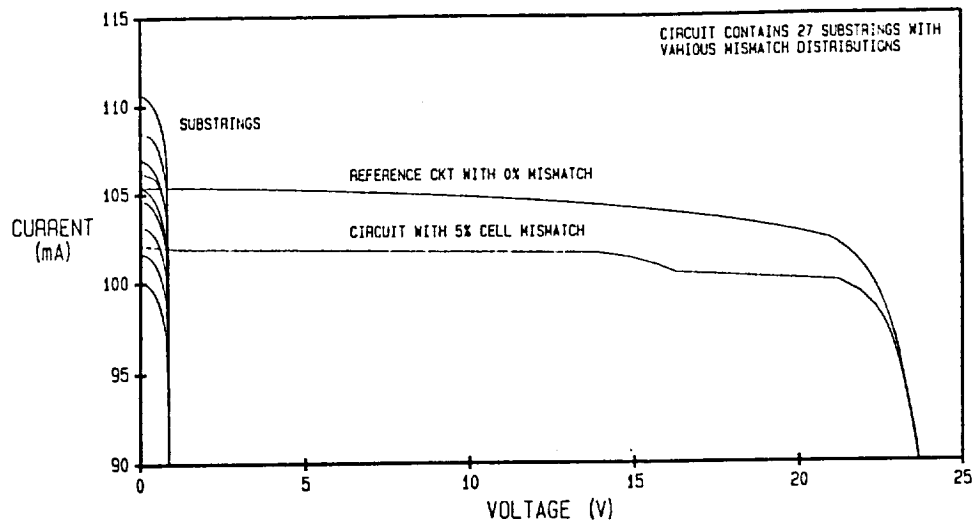


Figure 8. Circuit Sensitivity to Cell Mismatching

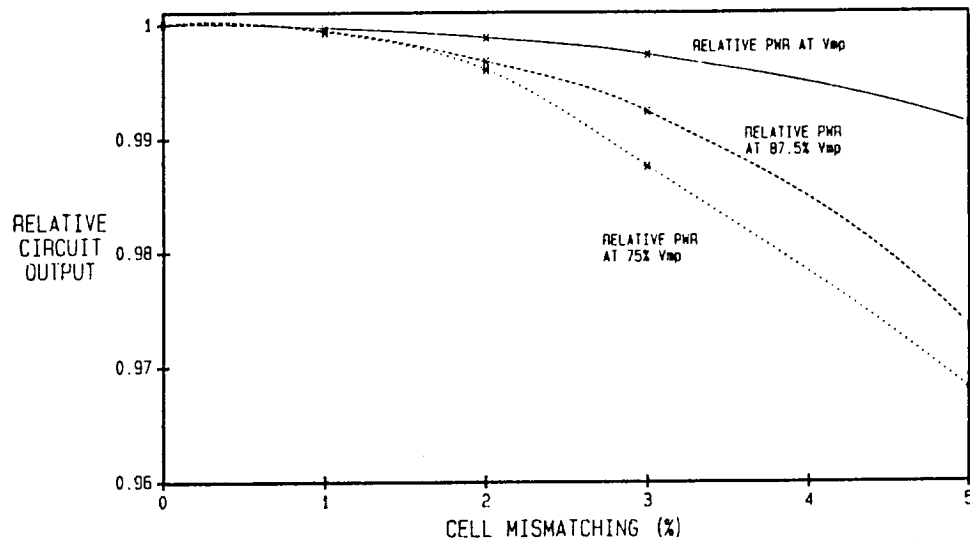


Figure 9. Relative Circuit Performance to Cell Mismatching

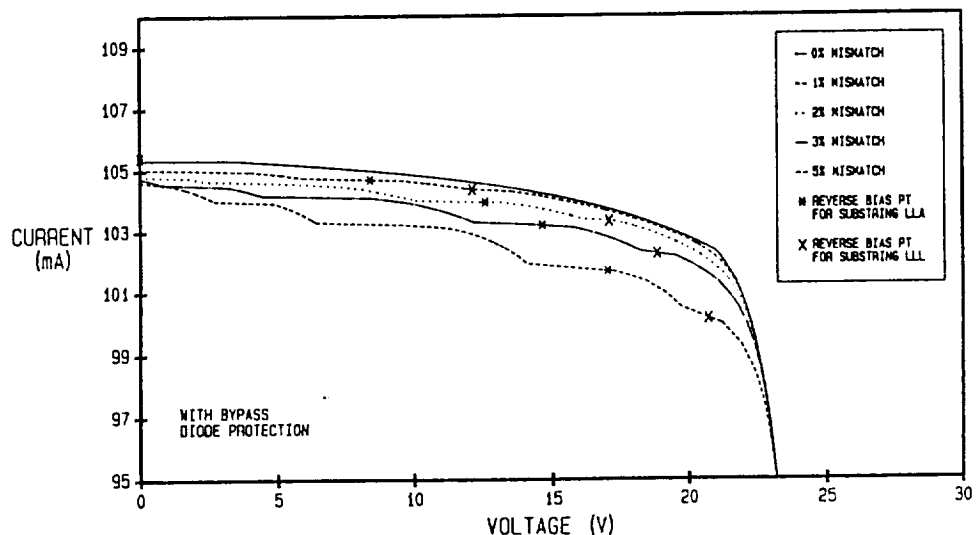


Figure 10. Bypass Diode Protected Circuit Sensitivity to Cell Mismatching

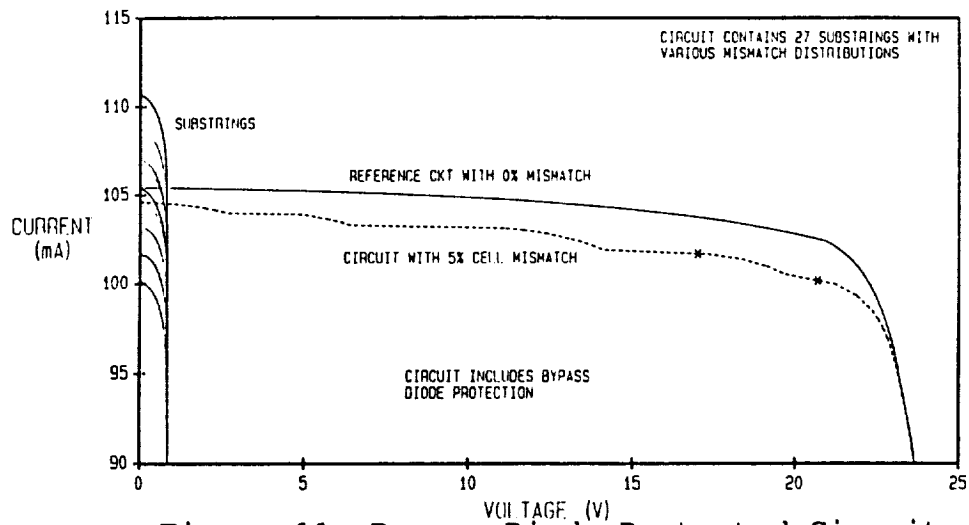


Figure 11. Bypass Diode Protected Circuit Sensitivity to Cell Mismatching

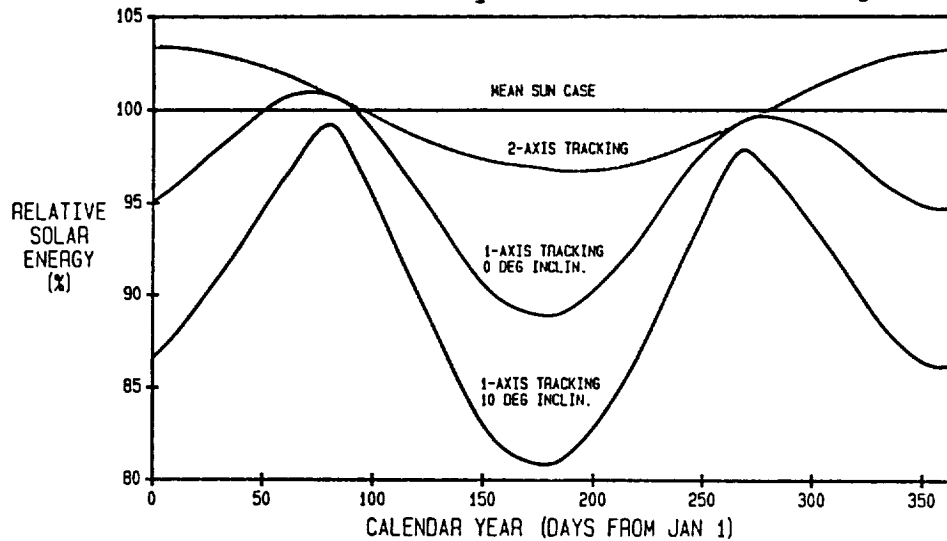


Figure 12. Seasonal Incident Solar Flux

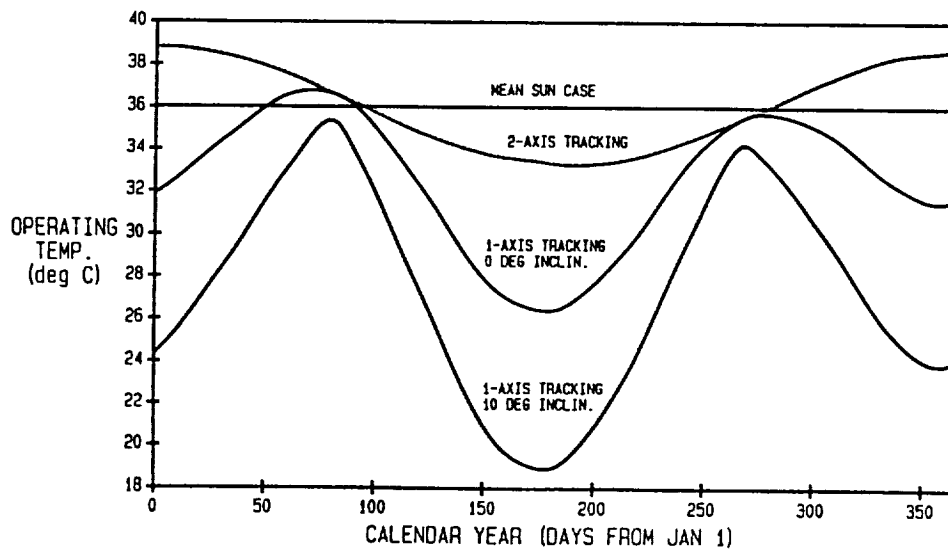


Figure 13. Seasonal Cell Module Operating Temperature

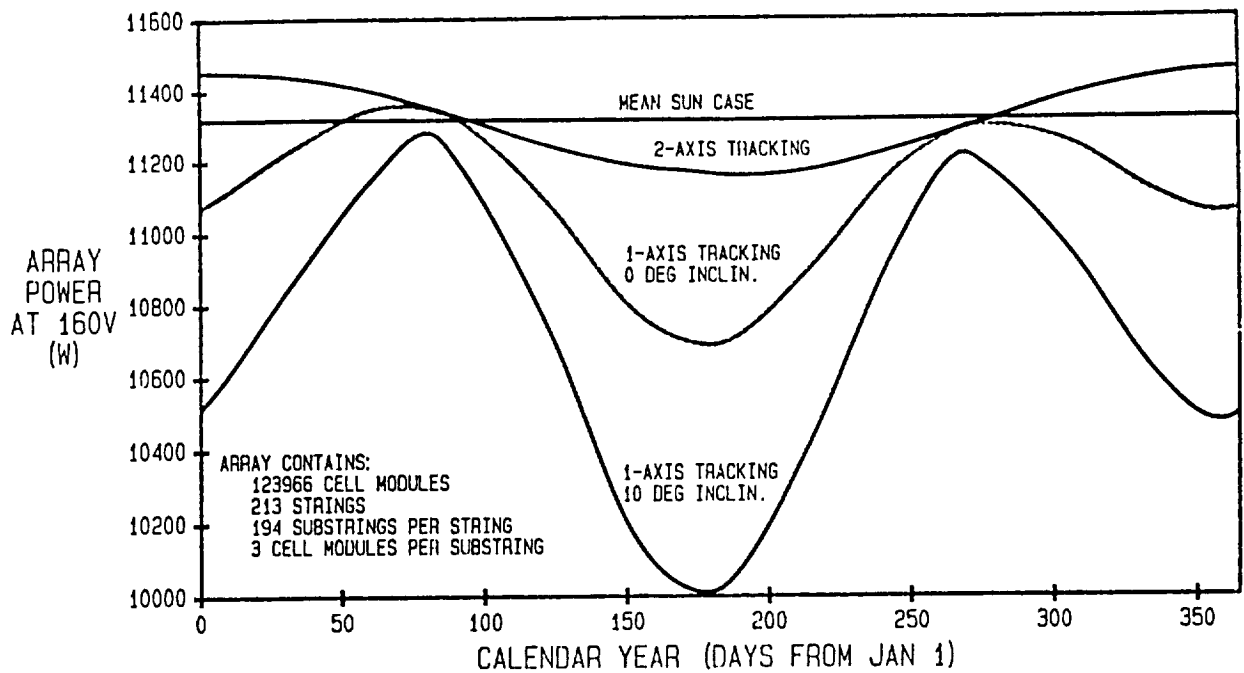


Figure 14. Seasonal Array Performance at Rated Voltage

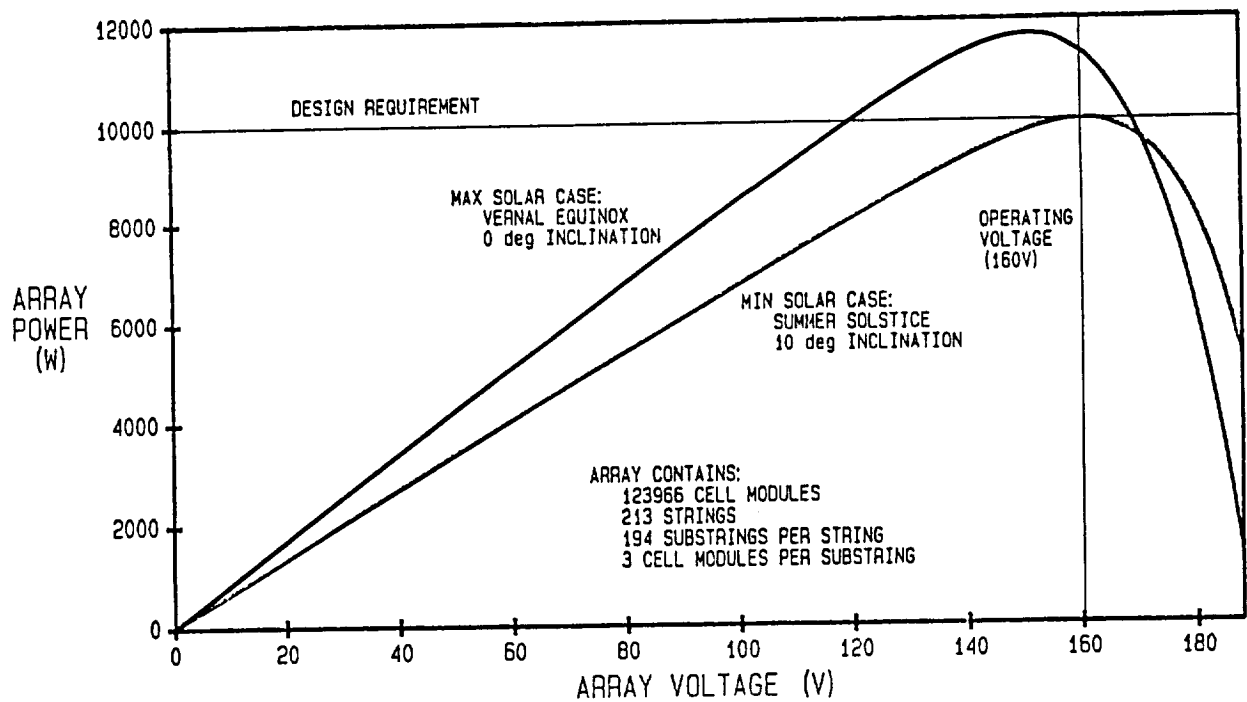


Figure 15. Minimum and Maximum BOL Array Performance